II. AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Previously Presented) A method for selectively scaling an integrated circuit design layout, the method comprising the steps of:

identifying a scaling target for at least two problem objects of the design layout based on feedback from a manufacturing process regarding problems caused by the problem objects in manufacturing an integrated circuit chip according to the design layout;

defining technology ground rules and methodology constraints for each problem object;

individually determining a scaling factor for each problem object without considering a scale factor of a different problem object of a same type as the problem object;

determining which at least one of a plurality of scaling techniques is to be applied to each problem object, and scaling each problem object with a respective at least one scaling technique and scaling factor; and

in a case that assembly is required, performing placement and routing to assemble the design using the scaled problem object.

2. (Previously Presented) The method of claim 1, wherein the at least two problem objects are selected from the group comprising: a layer, a region and a cell.

3. (Original) The method of claim 1, wherein the placement and routing performing step includes using an optimization-based hierarchical scaling program to produce a legal layout for each problem object.

4. (Original) The method of claim 1, wherein the scaling factor is at least one of: a compensation, a new ground rule and a scaling multiplier.

5. (Previously Presented) The method of claim 1, wherein the identifying step includes:

manufacturing the design layout;

testing the manufactured design layout and identifying at least two problem objects that are problems; and

generating manufacturing information.

6. (Previously Presented) The method of claim 5, wherein the testing step includes characterizing operation and identifying the at least two problem objects by obtaining data indicating how well objects are able to be manufactured.

7. (Original) The method of claim 5, wherein the manufacturing information generating step includes generating the scaling target for the problem object.

8. (Original) The method of claim 1, further comprising the step of evaluating whether a new design layout including the scaled objects achieves an expected behavior.

9-30. (Cancelled).

31. (Previously Presented) A method for selectively scaling an integrated circuit design layout, the method comprising the steps of:

identifying a scaling target for at least two problem objects of the design layout based on feedback from a manufacturing process regarding problems caused by the problem objects in manufacturing an integrated circuit chip according to the design layout;

defining technology ground rules and methodology constraints for each problem object;

individually determining a scaling factor for each problem object without considering a scale factor of a different problem object of a same type as the problem object;

determining which at least one of a plurality of scaling techniques is to be applied to each problem object, and scaling each problem object with a respective at least one scaling technique and scaling factor; and

in a case that assembly is required, performing placement and routing to assemble the design using the scaled problem object;

wherein the scaling factor includes at least one of a compensation and a new ground rule.

32. (Previously Presented) The method of claim 31, wherein the identifying step

includes:

manufacturing the design layout;

testing the manufactured design layout and identifying at least two problem objects that are problems; and

generating manufacturing information.

33-36. (Cancelled).